SCHEME OF INSTRUCTION & EXAMINATION
B.E. III- Semester
(ELECTRONICS AND TELECOMMUNICATION ENGINEERING)

S. No.	Course Code	Course Title	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/ D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
Theory Course										
1	HS 102 EG	Effective Technical Communication in English	3	-	-	3	30	70	3	3
2	HS 103 CM	Finance and Accounting	3	-	-	3	30	70	3	3
3	ES 303 ET	Digital Electronics	3	1	-	4	30	70	3	4
4	ES 304 ET	Probability Theory and Stochastic Processes	3	1	-	4	30	70	3	4
5	PC 401 ET	Electronic Devices	3	-	-	3	30	70	3	3
6	PC 402 ET	Network Theory	3	1	-	4	30	70	3	4
Practical/Laboratory Course										
7	PC 451 ET	Electronic Devices and Circuits Lab	-	-	2	2	25	50	3	1
8	PC 452 ET	Electronic Workshop	-	-	2	2	25	50	3	1
Total			**18**	**3**	**4**	**25**	**230**	**520**		**23**

PC: Professional Course **HS:** Humanities and Social Sciences **ES:** Engineering Science

L: Lecture **T:** Tutorial **P:** Practical **D:** Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination (Univ. Exam)

EG: English **CM:** Commerce
ET: Electronics and Tele Communication Engineering

Note:

1. Each contact hour is a Clock Hour
2. The duration of the practical class is two clock hours, however it can be extended wherever necessary, to enable the student to complete the experiment

EFFECTIVE TECHNICAL COMMUNICATION IN ENGLISH

HS 102 EG

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

1.Features of technical communication
2.Types of professional correspondence and Techniques of report writing
3. Basics of manual writing and Aspects of data transfer and presentations.

Outcomes: On successful completion of the course, the students would be able to

1.Handle technical communication effectively
2.Use different types of professional correspondence
3.Use various techniques of report writing
4.Acquire adequate skills of manual writing
5.Enhance their skills of information transfer and presentations

UNIT – I
***Definition and Features of Technical communication*:** Definition and features of technical communication(precision, relevance, format, style, use of visual aids), Differences between general writing and technical writing, Types of technical communication (oral and written)
UNIT – II
Technical Writing-I (Official correspondence): Emails, IOM, Business letters, Business proposals.
UNIT – III
Technical writing-II (Reports): Project report, Feasibility report, Progress report, Evaluation report.
UNIT – IV
Technical writing- III (Manuals): Types of manuals, User manual, Product manual, Operations manual.
UNIT – V
Information Transfer and Presentations: Non-verbal (bar diagram, flow chart, pie chart, tree diagram) to verbal (writing), Verbal (written) to non-verbal, Important aspects of oral and visual presentations.

Suggested Readings:

1.	Raman, Meenakshi & Sharma, Sangeeta. (2015). "*Technical Communication: Principles and Practice",* 3/e, New Delhi.
2.	Rizvi,Ashraf, M. (2017), "*Effective Technical Communication",* 2/e,Tata McGraw Hill Education. New Delhi.
3.	Tyagi, Kavita &Misra, Padma. (2011). "*Advanced Technical Communication",* New

	Delhi, PHI Learning.
4.	Sharma, R. C., & Mohan, Krishna. (2017). "*Business Correspondence and Report Writing: A Practical Approach to Business & Technical Communication",*4/e, Tata McGraw Hill Education. New Delhi.

FINANCE AND ACCOUNTING

HS 103 CM

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

1.To provide basic understanding of Financial and Accounting aspects of a business unit
2.To provide understanding of the accounting aspects of business and financial statements
3. To provide inputs necessary to evaluate the viability of projects and the skills necessary to analyse the financial statements

Outcomes: On successful completion of the course, the students would be able to

1. Evaluate the financial performance of the business unit.
2. Take decisions on selection of projects.
3. Take decisions on procurement of finances.
4. Analyse the liquidity, solvency and profitability of the business unit.
5. Evaluate the overall financial functioning of an enterprise.

UNIT – I
***Basics of Accounting*:** Financial Accounting–Definition- Accounting Cycle–Journal - Ledger and Trial Balance-Cash Book-Bank Reconciliation Statement (including Problems)
UNIT – II
Final Accounts: Trading Account-Concept of Gross Profit- Profit and Loss Account-Concept of Net Profit-Balance Sheet (including problems with minor adjustments)
UNIT – III
***Financial System and Markets*:** Financial System-Components-Role-Considerations of the investors and issuers- Role of Financial Intermediaries. Financial Markets-Players- Regulators and instruments - Money Markets Credit Market- Capital Market (Basics only)
UNIT – IV
***Basics of Capital Budgeting techniques*:** Time Value of money- Compounding- Discounting- Future Value of single and multiple flows- Present Value of single and multiple Flows- Present Value of annuities-Financial Appraisal of Projects– Payback Period, ARR- NPV, Benefit Cost Ratio, IRR (simple ratios).
UNIT – V
***Financial statement Analysis*:** Financial Statement Analysis- Importance-Users-Ratio Analysis-liquidity, solvency, turnover and profitability ratios.

Suggested Readings:

1	Satyanarayana. S.V. and Satish. D., "*Finance and Accounting for Engineering"*, Pearson Education.
2	Rajasekharan, "*Financial Accounting"*, Pearson Education.
3	Sharma.S.K. and Rachan Sareen, "*Financial Managemen"*, Sultan Chand.
4	Jonathan Berk, "*Fundamentals of Corporate Finance",* Pearson Education.
5	Sharan, "*Fundamentals of Financial Management"*, Pearson Education.

DIGITAL ELECTRONICS

ES 303 ET

Instruction: 3+1 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 4

Objectives:

1. To learn the principles of digital hardware and support given by it to the software.
2. To explain the operation and design of combinational and arithmetic logic circuits.
3. To design hardware for real world problems

Outcomes: On successful completion of the course, the students would be able to

1. Understand the deign process of digital hardware, use Boolean algebra to minimize the logical expressions and optimize the implementation of logical functions.
2.Understand the number representation and design combinational circuits like adders, MUX etc.
3. Design Combinational circuits using PLDS and write Verilog code for basic gates and combinational circuits.
4. Analyse sequential circuits using flip-flops and design registers, counters.
5.Represent a sequential circuit using Finite State machine and apply state minimization techniques to design a FSM

UNIT – I
Design Concepts: Digital Hardware, Design process, Design of digital hardware. Introduction to logic circuits – Variables and functions, Logic gates and networks. Boolean algebra, Synthesis using gates, Design examples. Optimized implementation of logic functions using K-Map and Quine-McCluskey Tabular method.
UNIT – II
Number representation: Addition and Subtraction of signed and unsigned numbers. ***Combinational circuit building blocks:*** Adders and Subtractors, Multiplexers. Demultiplexers, Parity Checkers and Generators, Decoders. Encoders. Code converters, BCD to 7-segment converter, Arithmetic comparator circuits. Verilog modeling of simple combination circuits.
UNIT – III
Design of combinational circuits using Programmable Logic Devices (PLDs): General structure of a Programmable Array Logic (PAL), Programmable Logic Arrays (PLAs), Structure of CPLDs and FPGAs, 2-input and 3-input lookup tables (LUTs).
UNIT – IV
Sequential Circuits: Basic Latch, Gated SR Latch, gated D Latch, Master-Slave edge triggered flip-flops, T Flip-flop, JK Flip-flop, Excitation tables. Registers and Counters. Verilog modeling of simple sequential circuits.
UNIT – V

***Synchronous Sequential Circuits*:** Basic Design Steps, Finite State machine(FSM) representation using Moore and Mealy state models, State minimization, Design of FSM for Sequence Generation and Detection, Algorithmic State Machine charts.

Suggested Readings:

1	Moris Mano and Michael D CIletti, "*Digital Design"*, Pearson, 4/e, 2008.
2	Zvi Kohavi, "*Switching and Finite Automata Theory"*, 3/e, Cambridge University Press-New Delhi, 2011.
3	R. P Jain, "*Modern Digital Electronics"*,4/e, McGraw Hill Education (India) Private Limited, 2003.
4	Ronald J.Tocci, Neal S. Widmer &Gregory L.Moss, "*Digital Systems: Principles and Application"*, PHI, 10/e, 2009.
5	Samir Palnitkar, "*Verilog HDL A Guide to Digital Design and Synthesis"*, 2/e, Pearson Education, 2006.

PROBABILITY THEORY AND STOCHASTIC PROCESSES

ES 304 ET

Instruction: 3+1 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 4

Objectives:

1. To understand fundamentals of probability and Random variables as applicable to Electronic Engg.
2.To learn one Random variable characteristic functions of different variables using their density functions
3.To understand elementary concepts of the Stochastic Processes and their temporal characteristics

Outcomes: On successful completion of the course, the students would be able to

1. understand different types of Random variables, their density and distribution functions
2. learn one Random variable characteristic functions of different variables using their density functions
3. extend the bi-variate distributions and the operations on them.
4. understand elementary concepts of the Stochastic Processes in the Temporal domain.
5. analyse the frequency domain information of Stochastic Processes

UNIT – I
***Concepts of Probability and Random Variable*:** Probability introduced through Set Theory and Operations – Definitions and Axioms, Causality versus Randomness, Borel Field, Probability Space – Discrete and Continuous, Events - Definition and independent events, Joint Probability, Conditional Probability, Repeated Trials, Combined Experiments, Bernoulli Trials, Bernoulli's Theorem, Total Probability, Baye's Theorem. **Random Variable:** Definition of a Random Variable, Conditions for a Function to be a Random Variable, Discrete, Continuous and Mixed Random Variables.
UNIT – II
Distribution & Density Functions and Operations on One Random Variable: Distribution and Density functions and their Properties - Binomial, Poisson, Uniform, Gaussian, Gamma, Rayleigh and Conditional Distribution, Methods of defining Conditional Event, Conditional Density, Properties. Expected Value of a Random Variable, Function of a Random Variable g(x) and its distribution, Moments about the Origin, Central Moments, Variance and Skew, Chebychev's Inequality (no proof), Characteristic Function, Moment Generating Function; Transformations of Random Variables
UNIT – III
Two Random Variables and operations Bi-variate Distributions, One Function of Two Random Variables, Two functions of two random variables, Joint Distribution and Density Function and their properties, Joint Moments, Joint Characteristic Functions, Conditional Distributions (Point & Interval), Conditional Expected Values. Central Limit Theorem (no

proof); Engineering application (theoretical discussion) – Mutual information, Channel Capacity and Channel Coding.
UNIT – IV
Stochastic Processes – Temporal Characteristics: Introduction to stationarity (First and Second order; WSS; SSS), statistical independence, Time averages and ergodicity, random processes and independence, Mean-Ergodic Processes, Correlation-Ergodic Processes, Autocorrelation Function and its Properties, Cross-Correlation Function and its Properties, Covariance and its Properties. Linear System Response of Mean and Mean-squared Value. Introduction to Gaussian and Poisson Random Processes.
UNIT – V
Stochastic Processes – Spectral Characteristics: Power Spectral Density and its properties; Relationship between Power Spectrum and Autocorrelation Function; Relationship between Cross-Power Spectrum and Cross-Correlation Function; White and colored noise, response to linear systems and stochastic inputs, concept of Markov Processes.

Suggested Readings:

1	Henry Stark and John W. Woods, "*Probability and Random Processes with Application to Signal Processing"*, 3/e, Pearson Education, 2014.
2	Athanasius Papoulis and S. Unnikrishna Pillai, "*Probability, Random Variables and Stochastic Processes"*, 4/e, McGraw Hill, 2006.
3	Peyton Z. Peebles, "*Probability, Random Variables & Random Signal Principles"*, 4/e, Tata McGraw Hill, 2001
4	P. Ramesh Babu, "*Probability Theory and Random Processes*", 1/e, McGraw Hill Education (India) Private Limited, 2015.
5	Gearge R. Cooper, Clave D.MC Gillem, "*Probability Methods of Signal and System Analysis"*, Oxford, 3/e, 1999.

ELECTRONIC DEVICES

PC 401 ET

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

1. Study semiconductor physics and Analyze the behavior of Semiconductor diodes in Forward and Reverse bias. Develop Half wave and Full wave rectifiers with L, C Filters.
2.Explain V-I characteristics of Bipolar Junction Transistor in CB, CE & CC configurations and Design DC Biasing techniques, evaluate A.C parameters for BJT in Amplifier Applications
3.Explore V-I characteristics of FETs, MOSFETs and study IC fabrication techniques

Outcomes: On successful completion of the course, the students would be able to

1. Interpret the characteristics and apply diode models to analyze various applications of diodes.
2. Identify the merits and demerits of various filters, formulate and design rectifier circuits with filters Calculate ripple factor, efficiency and percentage regulation of rectifier circuits.
3. Discriminate the BJT configurations to recognize appropriate transistor configuration for any given application and design the biasing circuits with good stability.
4. Analyze, Compare and design of BJT amplifiers with various biasing circuits.
5.Distinguish the working principles of BJT and FET also between FET & MOSFET

UNIT – I
Basics of Semiconductors*:** Energy bands in intrinsic and extrinsic Silicon. Carrier transport: diffusion current, drift current, mobility and resistivity; Generation and recombination of carriers, Poisson and continuity equation, Hall Effect ***Junction Diode: PN Junction formation, Characteristics, biasing–band diagram and current flow, Diode current equation, Breakdown in diodes, Diode as a circuit element, Small signal diode models, Diode switching characteristics, Zener Diode, Zener voltage regulator and its limitation, Schotky diode.
UNIT – II
PN Diode Applications: Half wave, Full wave and Bridge rectifiers–their operation, performance characteristics and analysis. Filters (L, C filters) used in power supplies and their ripple factor calculations, design of Rectifiers with and without Filters. ***Special Diodes****:* Elementary treatment on the functioning of Light Emitting diode, Photodiode and Solar cells.
UNIT – III
Bipolar Junction Transistor: Transistor Junction formation (collector-base, base-emitter Junctions),Transistor biasing – band diagram for NPN and PNP transistors, current components and current flow in BJT, Ebers moll model, Modes of transistor operation, BJT V-I characteristics in CB, CE, CC configurations, BJT as an amplifier, BJT biasing techniques, operating point stabilization against temperature and device variations, Bias stabilization and

compensation techniques, Biasing circuits design.
UNIT – IV
Small Signal Transistors equivalent circuits: Small signal low frequency h-parameter model of BJT, Approximate model, Analysis of BJT amplifiers using Approximate model for CB, CE and CC configurations; High frequency - Π model, Relationship between hybrid - Π and h – parameter model.
UNIT – V
Junction Field Effect Transistors (JFET): JFET formation, operation & current flow, V-I characteristics of JFET, Low frequency small signal model of FETs, Analysis of CS, CD and CG amplifiers. ***MOSFETs:*** Enhancement & Depletion mode MOSFETs, current equation, V-I characteristics, DC-biasing

Suggested Readings:

1	Jacob Millman, Christos C. Halkias, and Satyabrata Jit, "*Electronic Devices and Circuits"*, 3/e, McGraw Hill Education, 2010.
2	G. Streetman and S. K. Banerjee, "*Solid State Electronic Devices"*, 7/e, Pearson, 2014.
3	S. M. Sze and K. N. Kwok, "*Physics of Semiconductor Device"*, 3/e, John Wiley& Sons, 2006.
4	D. Neamen, D. Biswas, "*Semiconductor Physics and Devices"*, McGraw-Hill Education.
5	Robert Boylestad and Louis Nashelsky, "*Electronic Devices and Circuit Theory"*, 11/e, Pearson India Publications, 2015.

NETWORK THEORY

PC 402 ET

Instruction: 3+1 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 4

Objectives:

1. Concepts of Two Port networks, study about the different two port parameter representations.
2. Concepts about the image impedance on different networks, design of attenuators.
3. Design concepts of equalizers, different filters, network synthesis

Outcomes: On successful completion of the course, the students would be able to

1.Able to Express given Electrical Circuit in terms of A,B,C,D and Z,Y Parameter Model and Solve the circuits and how they are used in real time applications.
2. Able to learn how to calculate properties of networks and design of attenuators.
3. Able to design of equalizers.
4. Able to design different types of filters using passive elements.
5. Able to synthesize the RL & RC networks in Foster and Cauer Forms..

UNIT – I
Two Port networks: Z, Y, h, g and ABCD parameters, equivalence of two ports networks, T-π transforms, Reciprocity theorem, Interconnection of two port networks and Brune's test for inter connections.
UNIT – II
Symmetrical and Asymmetrical Networks: Characteristic impedance and propagation constant of symmetrical T and π networks, Image and iterative impedances, Image transfer constant and iterative transfer constant of asymmetrical L, T and π networks.
UNIT – III
***Constant k- Filters*-**Low pass, high pass, band pass and band elimination filter design, m-derived low pass and high pass filter design, Composite filter design and notch filter.
UNIT – IV
***Attenuators and Equalizers*-**Design of symmetrical T, π , Bridge-T and Lattice attenuators, impedance matching networks, Inverse networks, Equalizers, Constant resistance equalizer, full series and full shunt equalizer**.**
UNIT – V
Network Synthesis: Hurwitz polynomials, positive real functions, Basic Philosophy of Synthesis, L-C Immitance functions, RC impedance functions and RL admittance functions. RL impedance functions and RC admittance functions. Cauer and Foster's forms of RL impedance and RC admittance. Properties of RC, RL Networks**.**

Suggested Readings:

1	Ryder J.D, "*Network Lines Fields"*, 2/e, Prentice Hall of India,1991.
2	P.K. Jain and Gurbir Kau, "*Networks, Filters and Transmission Lines",* Tata McGraw-Hill Publishing Company Limited.
3	A. Sudhakar Shyammohan, "*Circuits Networks: Analysis Synthesis"*, 4/e, Tata McGraw-Hill, 2010.
4	Van Valkenburg M.E, "*Introduction to Modern Network Synthesis",* Wiley Eastern, 1994.
5	S.P. Ghosh and A.K. Chakraborty, "*Network Analysis and Synthesis",* McGraw Hill, 1/e, 2009.

ELECTRONIC DEVICES AND CIRCUITS LAB

PC 451 ET

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 25 marks *SEE: 50 marks*
Credits: 1

Objectives:

1.Study the characteristics of PN diode
2.Learn the characteristics of BJT in CE, CB and CC configurations and Plot the characteristics of FET in CS and CD configurations
3.Observe the parameters of BJT and FET amplifiers and Design biasing circuits

Outcomes: On successful completion of the course, the students would be able to

1.Understand characteristics of Diodes
2. Plot the characteristics of BJT in different configurations.
3. Record the parameters of BJT and FET amplifiers.
4. Understand biasing techniques of BJT.
5. Use the SPICE software for simulating electronic circuits.

List of Experiments

1. V-I Characteristics of Silicon and Germanium diodes and measurement of static and dynamic resistances.
2. Zener diode Characteristics and its application as voltage regulator.
3. Design, realization and performance evaluation of half wave rectifiers without and with filters.
4. Design, realization and performance evaluation of full wave rectifiers without and with filters.
5. V-I Characteristics of BJT in CB configuration.
6. V-I Characteristics of BJT in CE configuration.
7. V-I Characteristics of JFET in CS configuration.
8. Frequency response of Common Emitter BJT amplifier.
9. Frequency response of Common Source FET amplifier.
10. BJT Biasing circuit design.
11. V-I characteristics of UJT
12. Simulate any four experiments using PSPICE

Note: A minimum of 10 experiments should be performed

ELECTRONIC WORKSHOP

PC 452 ET

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 25 marks *SEE: 50 marks*
Credits: 1

Objectives:

1.To learn the usage of basic electronic components, equipment and meters used in electronic Laboratories and To learn practical electric AC and DC circuits
2.Verify the truth tables of combinational and sequential circuits
3.Realize combinational and sequential circuits and Design adder / subtractor

Outcomes: On successful completion of the course, the students would be able to

1. Use the basic electronic components and design circuits.
2. Verify various parameters of the circuits by applying theorems.
3. Understand the pin configuration of ICs and verify the operation of basic gates
4. Design and verify the combinational and logic circuits.
5. Use the SPICE software for simulating circuits.

List of Experiments

Part A

1. Study of all types of discrete Active & passive devices, display devices, integrated components, electro mechanical components (switches, sockets, connectors etc.,) electromagnetic components (relays). Study and use of different meters (volt/ammeter, AVO/Multi meter) for the measurement of electrical parameters. Measurement of RLC components using LCR Meter.
2. Soldering and Desoldering
3. PCB design and circuit assembling
4. Study of CRO and its applications.
5. Design and Verification of Superposition and Tellegan's theorem
6. Design and Verification of Thevenin's and Maximum Power Transfer Theorem.
7. Measurement of two-port network parameters.
8. Measurement of Image impedance and Characteristics impedance.

Part B

Implement using digital ICs

9. Verification of truth tables of Logic gates and realization of Binary to Gray and Gray to Binary code converters.
10. Realization of Half adder/sub and full adder/sub using universal logic gates.
11. Realization of Full adder/Sub using MUX and Decoder
12. Design 2's complement Adder/subtractor using IC 74283 and verify experimentally.
13. Verification of truth tables of Flip Flops and Flip flop conversions form one form to the other.

Note: A minimum of 6 experiments in Part-A and 4 experiments in Part-B should be performed. The students may use any commercial / open source SPICE programs available like MULTISIM, PSPICE, TINA, and LAB VIEW for simulation.