SCHEME OF INSTRUCTION & EXAMINATION
B.E.VI-Semester
(ELECTRONICS AND COMMUNICATIONENGINEERING)

S.No.	Course Code	Course Title	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration inHrs	
Theory Course										
1	PC413EC	Digital Communication	3	-	-	3	30	70	3	3
2	PC414EC	VLSI Design	3	-	-	3	30	70	3	3
3	PC415EC	Data Communication and Computer Networks	3	-	-	3	30	70	3	3
4	PE5XXEC	Professional Elective-I	3	-	-	3	30	70	3	3
5	PE5XXEC	Professional Elective-II	3	-	-	3	30	70	3	3
6	OE6XXYY	Open Elective-I	3	-	-	3	30	70	3	3
Practical/Laboratory Course										
7	PC458EC	Communication Systems Lab	-	-	2	2	25	50	3	1
8	PC459EC	Digital Integrated Circuits Lab	-	-	2	2	25	50	3	1
9	PC460EC	Data Communication and Computer Networks Lab	-	-	2	2	25	50	3	1
*10	*PW701EC	*Summer Internship	-	-	-	-	*50		-	*2
Total			**18**	**-**	**6**	**24**	**255**	**570**	**27**	**21**

PC: Professional Core **PE:** Professional Elective
OE: Open Elective **PW:** Project Work
L:Lecture **T:**Tutorial **P:**Practical
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination(Univ.Exam)
EC: Electronics and Communication Engineering

Note:

1. Each contact hour is a clock hour.
2. The duration of the practical class is two clock hours, however it can be extended wherever necessary,to enable the student to complete the experiment.
3. *The students have to undergo a Summer Internship of four to six weeks duration after VI semester and credits will be awarded in VII semester after evaluation.

Professional Elective-I		
S. No.	**Course Code**	**Course Title**
1	PE501EC	Digital Image and Video Processing
2	PE502EC	Advanced Microcontrollers
3	PE503EC	Python Programming and Applications
4	PE504EC	Neural Networks

Professional Elective-II		
S.No.	**Course Code**	**Course Title**
1	PE505EC	FPGA Architectures
2	PE506EC	Advanced Digital Signal Processing
3	PE507EC	CMOS Analog IC Design
4	PE508EC	IoT system Design and Applications

Open Elective-I		
S. No.	**Course Code**	**Course Title**
1	OE611AE	Basics of Automobile Engineering(Not for Mech./Prod./Automobile Engg. students)
2	OE601CE	Disaster Mitigation(Not for Civil Engg. Students)
3	OE601CS	Operating Systems(Not for CSE Students)
4	OE602CS	OOP using Java(Not for CSE Students)
5	OE601EE	Electrical Energy Conservation and Safety(Not for EEE & EIE Students)
6	OE602EE	Reliability Engineering(Not for EEE&EIE Students)
7	OE601EG	Soft Skills & Interpersonal Skills
8	OE601IT	Database Systems(Not for IT Students)
9	OE602IT	Data Structures(Not for IT Students)
10	OE601LW	Cyber Law and Ethics
11	OE611ME	Industrial Robotics (Not for Mech./Prod./Automobile Engg. students)
12	OE602MB	Human Resource Development and Organizational Behaviour
13	OE601EC	Principles of Electronic Communication(Not for ECE students)
14	OE602EC	Digital System Design using Verilog HDL(Not for ECE Students)

DIGITAL COMMUNICATION

PC413EC

Instruction:3periodsperweek *Duration of SEE:3 hours*
CIE:30marks *SEE:70 marks*
Credits: 3
Prerequisites:Probability Theory and Stochastic Processes (ES304ES)
Analog Communication (PC410EC)

Course Objectives:

1. To introduce the concepts of optimum receiver, baseband digital data transmission and analyze the error performance of different digital carrier modulation schemes like ASK, FSK, PSK etc.
2. To familiarize the students with the concepts of information theory, basic source coding and channel coding techniques.
3. To familiarize the students with the concepts of spread spectrum communication with emphasis on DSSS and FHSS.

Course Outcomes: On successful completion of the course, the students will be able to

1. understand the design of optimum receiver and analyze the Performance of Baseband and Band pass Modulation schemes based on Probability of error.
2. apply concepts of Information theory and assess information capacity of various channels.
3. encode the source alphabet using Shannon Fano and Huffman encoding methods.
4. distinguish different types of Error control codes along with their encoding/decoding algorithms.
5. understand generation of PN sequence and analyze the performance of Spread Spectrum communication systems.

UNIT– I
Introduction to Digital Communication: Elements of Digital Communication System**,** Comparison of Digital and Analog Communication Systems. **Detection and Estimation:** Receiver structure,Detection of signals in the presence of noise - Gaussian error probability, optimum receiver – matched filter, Gram-Schmidt orthogonalization procedure, correlation receiver, Maximum Likelihood decoding. **Base band digital data transmission –** Block diagram, Inter Symbol Interference, Nyquist criterion for Zero ISI, Eye pattern.
UNIT– II
Digital Carrier Modulation Schemes — Description and generation of ASK, FSK, PSK. Signal Constellation, Coherent detection of Binary ASK, FSK, PSK. DPSK. Comparison of digital carrier modulation schemes. **M-arysignaling schemes:** Introduction, QPSK- generation and detection, Signal Constellation, Synchronization methods.
UNIT– III
Information Theory and Source Coding: Uncertainty, Information, entropy, information rate.. Discrete memory less channel – Probability relations in a channel, priori & posteriori entropies, Joint entropy, conditional entropy, mutual information, Channel capacity - Binary Symmetric Channel, Binary Erasure Channel, cascaded channels, Shannon-Hartley Theorem – Shannon

Bound. **Source coding:** Shannon – Fano and Huffman coding.
UNIT– IV
Channel Coding: Introduction to error correcting codes,types of transmission errors, need for error control coding. **Linear Block Codes (LBC):** Matrix description of LBC, generation, Syndrome calculation and error detection, Minimum distance of Linear block code, error detection and error correction capabilities, Hamming codes. **Binary cyclic codes (BCC):** Polynomials, Algebraic description of cyclic codes, systematic encoding using generator polynomial and parity check polynomial, syndrome calculation, decoding and error correction using shift registers. **Convolution codes:** Encoding, Decoding using code tree, state diagram.
UNIT– V
Spread Spectrum Communication: Advantages of Spread Spectrum, generation and characteristics of PN sequences. Direct sequence spread spectrum and Frequency hopping spread spectrum systems. CDMA, ranging using DSSS. Acquisition and Tracking of DSSS and FHSS signals.

SuggestedReading:

1	Simon Haykin, “Digital Communication”, 4th edition, Wiley India 2011.
2	Sam Shanmugam K, “Digital and Analog Communication systems”, Wiley 1979.
3	B.P.Lathi, “Modern digital and analog communication systems”, 3rd edition, Oxford University Press. 1998.
4	Leon W.Couch II., “Digital and Analog Communication Systems”, 6th edition, Pearson Education inc., New Delhi, 2001.
5	H. Taub, D.L. Schilling, “Principles of communication systems”, Tata McGraw Hill, 2001.

VLSI DESIGN

PC414EC

Instruction: 3 periods per week *Duration of SEE:- 3hours*
CIE: 30 marks *SEE:- 70 Marks*
Credits: 3
Prerequisites: Digital Electronics (ES215EC)

Course Objectives:

1. To explain electrical properties of MOS devices to analyze the behavior of inverters designed with various loads.
2. To give exposure to the design rules to be followed to draw the layout of any logic circuit and Provide concept to design different types of Combinational and sequential circuits
3. To describe verilog HDL and develop digital circuits using various modeling styles.

Course Outcomes: On successful completion of the course, the students will be able to

1. analyze modes of operation of MOS transistor and its basic electrical properties.
2. draw stick diagrams and layouts for any MOS transistors and calculate the parasitic R&C
3. familiarize with the constructs and conventions of the verilog HDL programming in gate level and data flow modeling.
4. generalize combinational and sequential logic circuits in behavioral modeling and concepts of switch level modelling.
5. analyse the operation of various arithmetic and sequential logic circuits using CMOS transistors

UNIT I
Introduction: Introduction to IC Technology – MOS, PMOS, NMOS, CMOS Fabrication Process. **Basic Electrical Properties**: Basic Electrical Properties of MOS: Ids- Vds relationships, MOS transistor threshold Voltage, gm, gds, figure of merit; Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design.
UNIT –II
VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates. Basic circuit concepts, Sheet Resistance R_S and its concept to MOS, Area Capacitance Units, Calculations – RC Delays.
UNIT- III
Introduction to HDLs: Basic Concepts of Verilog, Data types, system tasks and compiler directives. Gate level modeling: Gate types and gate delays, dataflow modeling: Continuous assignments and Delays. Design of stimulus blocks. Design of Arithmetic Circuits using Gate level/ Data flow modeling –Adders, Subtractors, 4- bit Binary and BCD adders and 8-bit Comparators.
UNIT – IV
Behavioral modeling: Structured Procedures, Procedural Assignments, Timing Control, Conditional Statements, Sequential and parallel blocks, generate Blocks, Switch level modeling. Behavioral modeling of sequential logic modules: Latches, Flip Flops, counters and shift registers applications Tasks, Functions, Procedural Continuous Assignments, Design of Mealy and Moore FSM models for sequence detector using Verilog. Logic Synthesis, Synthesis Design Flow, Gate level netlist.

UNIT –V
Subsystem Design: Shifters, Carry skip adder, carry select adder , Booth Multiplier, Memory Elements: 6T SRAM cell, 1T DRAM cell. **Sequential Logic Design**: Behavior of Bi-stable elements, CMOS D latch and Edge triggered Flip flops.

Suggested Reading:

1.	Kamran EshraghianDougles and A. Pucknell, 'Essentials of VLSI circuits and systems', PHI, 2005Edition
2.	Weste and Eshraghian 'Principles of CMOS VLSI Design', Pearson Education, 2nd edition,1999.
3.	John .P. Uyemura, 'Introduction to VLSI Circuits and Systems', JohnWiley, 2003
4.	John M. Rabaey, 'Digital Integrated Circuits', PHI, EEE, 1997.
5.	Wayne Wolf, 'Modern VLSI Design', Pearson Education, 3rd edition, 1997

DATA COMMUNICATION AND COMPUTER NETWORKS

PC415EC

Instruction: 3 periodsperweek *Duration of SEE: 3 hours*
CIE:30 marks *SEE: 70marks*
Credits: 3
Prerequisites: Digital Electronics(ES215EC)
Analog Communication (PC410EC)

Course Objectives:

1. To understand concepts of switched communication networks and functions of each layer of OSI model for layered architecture and introduce TCP/IP suite of protocols.
2. To understand performance of data link layer protocol for flow and error control.
3. To understand different routing protocols, and various networked applications such as DNS, FTP, www architecture and network security.

Course Outcomes: On successful completion of the course, the students will be able to

1.	study function of layers in OSI model and understand various network topologies.
2.	understand network layer protocols, IP addressing and internetworking.
3.	understand transport layer working with TCP, and UDP.
4.	understand functionality of application layer and its protocols
5.	understand the importance of network security principles.

UNIT-I
Introduction to Data communication: A Communication Model, The Need for Protocol Architecture and Standardization, Network Types: LAN, WAN, MAN. Network Topologies: Bus, Star, Ring, Hybrid, Line configurations. Reference Models: OSI, TCP/IP. Transmission modes, DTE-DCE Interface, Transmission media- Guided media, Unguided media, Circuit Switching principles and concepts, Virtual circuit and Datagram subnets.
UNIT-II
Data Link Layer: Need for Data Link Control, Design issues, Framing, Error Detection and Correction, Flow control Protocols: Stop and Wait, Sliding Window, ARQ Protocols, HDLC. MAC Sub Layer: Multiple Access Protocols: ALOHA, CSMA, LAN- IEEE 802.2, 802.3, Wireless LAN- 802.11, 802.15, 802.16 standards. Bridges and Routers.
UNIT-III
Network Layer: Network layer Services, Routing algorithms: Shortest Path Routing, Flooding, Hierarchical routing, Broadcast, Multicast, Distance Vector Routing, and Congestion Control Algorithms. Internet Working: The Network Layer in Internet: IPV4, IPV6, Comparison of IPV4 and IPV6, IP Addressing.
UNIT-IV
Transport Layer: Transport Services, Elements of Transport Layer, Connection management, TCP and UDP protocols, ATM AAL Layer Protocol.
UNIT-V
Application Layer: Domain Name System, SNMP, Electronic Mail, World Wide Web. **Network Security**: Cryptography Symmetric Key and Public Key algorithms, Digital Signatures, Authentication Protocols.

Suggested Reading:

1.	Behrouz A. Forouzan, “Data Communication and Networking,”3/e, TMH, 2008.
2.	William Stallings, “Data and Computer Communications,” 8/e, PHI, 2004.
3.	Andrew S Tanenbaum, “Computer Networks,” 5/e, Pearson Education, 2011.
4.	Douglas E Comer, “Computer Networks and Internet”, 5/e, Pearson Education Asia, 2009.
5.	Prakash C. Gupta, “Data Communications and Computer Networks”, 2/e, PHI learning, 2013.

PROFESSIONAL ELECTIVE-I

DIGITAL IMAGE AND VIDEO PROROCESSING

PE501EC

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3
Prerequisites: Digital Signal Processing(PC408EC)

Course Objectives:

1. To provide an introduction to the basic concepts and methodologies for Digital Image and Video processing.
2. To acquaint with spatial and transform domain techniques used in Image Enhancement and to gain knowledge about various Image compression and segmentation methods.
3. To study applications of motion estimation in video processing.

Course Outcomes: On successful completion of the course, the students will be able to

1. develop a foundation that can be used as the basis for higher study and research in the Image and Video processing areas.
2. design various filters for processing of images without destroying fine details like edges and lines.
3. apply image processing techniques for processing and analysis of remotely sensed, Microscope, Radar and Medical images
4. understand the requirement for various image and video compression algorithms.
5. understand and analyze the performance of block matching algorithms in video coding standards.

UNIT – I
Fundamentals of Image Processing: Basic steps in Image Processing, Sampling and Quantization of an image, Relationship between pixels. **Image Transforms**: 2D- Discrete Fourier Transform, Discrete Cosine Transform, Haar Transform and Hoteling Transform.
UNIT – II
Image Processing Techniques: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. **Frequency domain methods:** Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.
UNIT – III
Image Compression: Functional Block diagram of a general image compression system, Various types of redundancies, Huffman coding, Arithmetic coding. **Segmentation:** Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.
UNIT – IV
Basic concepts of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image formation, sampling of video signals, filtering operations.
UNIT – V
2-D Motion Estimation: Optical flow, Pixel Based Motion Estimation, Block Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, multi resolution motion estimation. Application of motion estimation in Video coding.

Suggested Reading:

1. Rafael C. Gonzalez, Richard E. Woods, Digital Image Processing', Pearson Education, 2009, 3rd edition.
2. Yao Wang, Joern Ostermann, Ya-quin Zhang, 'Video processing and Communication', 1st edition, Prentice Hall International.
3. Vipul Singh, 'Digital Image Processing with MATLAB and Lab view', Elsevier 2013.
4. Anil K Jain, 'Fundamentals of Digital Image Processing', Prentice-Hall of India Private Limited, New Delhi, 1995.
5. M. Tekalp,'Digital Video Processing', Prentice Hall International,1995.

ADVANCED MICROCONTROLLERS

PE502EC

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3
Prerequisites: Microprocessor & Microcontroller (PC409EC)

Course Objectives:

1. To describe industry standard ARM microcontroller architecture.
2. To explain ability of programming ARM using Assembly language and Embedded C.
3. To discuss the Bus Architecture of ARM microcontroller.

Course Outcomes: On successful completion of the course, the students will be able to

1. illustrate the basic architecture of ARM.
2. analyse the instruction set of ARM and thumb instructions.
3. understand basic Embedded C concepts and multitasking.
4. program and interface the ARM with peripheral devices using Assembly Language and C.
5. understand the advance microprocessor bus architecture (AMBA).

UNIT – I

Introduction:
Introduction to advanced microcontrollers, Difference between RISC and CISC architectures, Endianness (Little and Big), Design philosophy of RISC and ARM architectures. History of ARM microprocessor, ARM processor family, Development of ARM architecture.

The ARM Architecture and Programmers' Model:
The Acorn RISC Machine, ARM core data flow model, architectural inheritance, The ARM7 TDMI programmer's model: General purpose registers, CPSR, SPSR, ARM memory map, data format, load and store architecture, Core extensions, Architecture revisions, ARM development tools.

UNIT – II

ARM Instruction Set: Data processing instructions, Arithmetic and logical instructions, Rotate and barrel shifter, Branch instructions, Load and store instructions, Software interrupt instructions, Program status register instructions, Conditional execution, Multiple register load and store instructions, Stack instructions, Thumb instruction set, advantage of thumb instructions, Assembler rules and directives.

UNIT – III

Basics of Embedded C : Overview of C compiler and optimization, Basic data types, Looping and branching, Register allocations, function calls, pointer aliasing, structure arrangement, bit fields, unaligned data, Division, floating point, Inline functions and inline assembly, Portability issues, Multitasking.

UNIT – IV

Assembly and C Programming for ARM: Assembly language programs for shifting of data, factorial calculation, swapping register contents, moving values between integer and floating point registers.

C programs for General purpose I/O, general purpose timer, PWM Modulator, UART, I2C Interface, SPI Interface, ADC, DAC.

UNIT – V

Advanced Microprocessor Bus Architecture (AMBA): Advanced Microprocessor Bus Architecture (AMBA), AMBA Bus System, User peripherals, Exception handling in ARM, and ARM optimization techniques.

Suggested Reading:

1.	Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM Systems Developer's Guide: Designing & Optimizing System Software", Elsevier, 2004.
2.	Muhammad Ali Mazidi, "ARM Assembly Language Programming & Architecture", Kindle Edition, 2013.
3.	William Hohl, Christopher Hinds, "Arm Assembly Language: Fundamentals and Techniques", 2nd Edition, CRC Press, 2014.
4.	Michael J. Pont, "Embedded C", Pearson Education India, 1st Edition, 2007.
5.	Dr.Yifeng Zhu, "Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C", E-Man Press LLC, 3rd Edition, 2017.

PYTHON PROGRAMMING AND APPLICATIONS

PE503EC
Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3
Prerequisites: Network Theory (PC402C), Signals and Systems(PC405EC)

Course Objectives:

1. To acquire programming skills by learning Syntax, Semantics and Regular expressions in core Python.
2. To analyse electronic circuits and examine the various signal transformation techniques using Python
3. To build IoT solutions using MicroPython running on small, dedicated microcontroller boards

Course Outcomes: On successful completion of the course, the students will be able to

1. build basic programs using fundamental programming constructs like variables, conditional logic, looping, and functions
2. examine Python syntax and semantics and be fluent in the use of Python flow control and functions.
3. create, run and manipulate Python Programs using core data structures like Lists, dictionaries and use Regular Expressions
4. develop programs in Python for implementation of non-linear circuits and analyze filters.
5. program their own IoT solutions in Python using MicroPython on small microcontroller boards.

UNIT-I
Introduction to Python: History of Python, Need of Python programming, Features of python, Python basics: Tokens, working with data types and variables, working with numeric data, working with string data, Python functions, Boolean expressions, selection structure, iteration structure **Functions:** default values of arguments, named arguments, local and global variables, **Modules**: creating, documenting and Importing modules, Use of standard modules.
UNIT-II
Lists:basic lists,creating and processing list of lists, Tuples, Dictionaries **Data structures**: Implementation of stacks and sets, binary search trees, Graph searching, working on sequences- reversing, permuting, sorting, Data Visualization: Different types of charts and graphs, selection of correct data visualization elements, software and tools available for data visualization.
Unit-III
Python Installation and Packages: Introduction to PIP, installing and uninstalling packages via PIP, Using python Packages: Numpy, Matplotlib, Scipy. **Circuit analysis**: Operations on vectors and matrices, Circuit representation, processing of components, Data structures of components, Introduction to Nodes, Branches and Loops, Loop and Nodal analysis. **Case study**: Model circuits and perform nodal analysis and loop analysis using **Lcapy(**open-source) Python package for solving linear circuits using matrix operations.
Unit- IV
Signal Analysis: Representation Continuous time signals, Discrete time signals, Python Implementation of sampling, Fourier Transform, Laplace transform, Z-transform, Discrete

Fourier Transform, Fast Fourier transform, Design of LTI filters, FIR filters and IIR filters using Python **Case study:** Cleaning Up Data Noise with Fourier Transform using Python
Unit-V
MicroPython : Introduction, Installing and running MicroPython, **Pyboard**- Architectural overview and Networking, hardware features of BBCmicro:bit, Overview of MicroPython libraries **Case study:** Traffic light simulation using MicroPython

Suggested Reading:

1.	Michael Urban and Joel Murach, "Python Programming", Mike Murach& Associates, Incorporated, 2016.
2.	Kalilur Rahman, "Python Data Visualization Essentials Guide", BPB publications,2021.
3.	Shivkumar V. Iyer , " Simulating Nonlinear Circuits with Python Power Electronics-An Open-Source Simulator, Based on Python, Springer International Publishing, 2018.
4.	Thomas Haslwanter, "Hands-on Signal Analysis with Python: An Introduction",Springer International Publishing, 2021.
5.	*Charles Bell, "MicroPython for the Internet of Things A Beginner's Guide to Programming with Python on Microcontrollers", Apress, 2017*

NEURAL NETWORKS

PE501EC

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3
Prerequisites:Probability Theory and Stochastic Processes (ES304ES)

Course Objectives:

1. To understand the functioning of biological neuron and its electronic implementation using different neuron models
2. To acquire knowledge on learning algorithms, architecture of deep learning, CNN and transfer learning.
3. To implement simple neural network using python programming.

Course Outcomes: On successful completion of the course, the students will be able to

1. differentiate between biological neuron & artificial neuron and different neuron models
2. apply learning algorithms and different feed forward neural networks
3. understand deep learning concepts and its architectures.
4. learn concepts of CNN and transfer learning techniques.
5. develop programs in Python for implementation of neural networks models

UNIT – I
Introduction to Neural Networks: Description of Biological Neuron, Mathematical model of Artificial Neural Network, Classification of Neural Networks, Different Neuron models: McCulloch-Pitts Neuron model, Perceptron Neuron model and ADALINE Neuron model, Basic learning laws.
UNIT – II
Neural Networks Algorithms: Learning algorithms, Maximum likelihood estimation, Building machine learning algorithm, Neural Networks Multilayer Perceptron, Back-propagation algorithm and its variants Stochastic gradient decent, Curse of Dimensionality.
UNIT – III
Introduction to Deep Learning & Architectures: Machine Learning Vs. Deep Learning, Representation Learning, Width Vs. Depth of Neural Networks, Activation Functions: Sigmoid, RELU, LRELU, ERELU, Tanh. Unsupervised Training of Neural Networks, Restricted Boltzmann Machines, Autoencoders.
UNIT – IV
Convolution Neural Networks: Architectural Overview – Motivation - Layers – Filters – Parameter sharing – Regularization, Popular CNN Architectures: ResNet, AlexNet . Transfer learning Techniques, Variants of CNN: DenseNet, PixelNet.
UNIT – V
Python programming: Python basics, Arrays and array operations, Functions and Files, Simple implementation of Artificial Neural Network, Classification with Multilayer Perceptron using Scikit-learn (MNIST Dataset).

Suggested Reading:

1.	B. Yeganaranarana, "Artificial Neural Networks", Eleventh EditionPrentice Hall, New Delhi, 2007.
2.	Ian Goodfellow, YoshuaBengio and Aaron Courville, "Deep Learning", MIT Press, 2017.
3.	Subir Varma and Sanjiv Das," Deep Learning" , 1st Edition, Published by Bookdown , 2018.
4.	*Umberto Michelucci "Applied Deep Learning. A Case-based Approach to Understanding Deep Neural Networks" Apress, 2018.*
5.	Ahmed Gad and Fatima Jarmouni, "Introduction to Deep Learning and Neural Networks with Python," A Practical Guide by Elsevier 1st Edition, 2020.

PROFESSIONAL ELECTIVE-II

FPGA Architectures

PE505EC

Instruction:3periodsperweek *Duration of SEE:3 hours*
CIE:30marks *SEE:70 marks*
Credits: 3
Prerequisites: Digital Electronics (ES303EC)

Objectives:

1. To discuss about Application Specific IC(ASIC)fundamentals and FPGA
2. To describe the power consumption in IC design
3. To discuss about the interconnection, placement and routing, verification and testing schemes.

Outcomes: On successful completion of the course, the students will be able to

1. understandthedesignflowofASICsandidentifytheimplementationtoolsrequiredforsimulationandsynthesisof FPGA Design.
2. demonstrate the architecture of FPGAs.
3. Explain the physical design of FPGAs and CAD tools for low level design entry.
4. Identify the placement & routing algorithms.
5. Validate the digital design and analyse the general design issues.

UNIT– I
Introduction to ASICs: TypesofASICs,ASICdesignflow,EconomiesofASIC's,Programmable ASICs: CPLD and FPGA. Commercially available CPLDs and FPGAs: XILINX,ALTERA,ACTEL.FPGADesigncycle,Implementationtools:Simulationandsynthesis,Programmingtechnologies.Applicationsof FPGAs.
UNIT– II
FPGA logic cell for XILINX, ALTERA and ACTEL ACT, Technology trends, Programmable I/Oblocks,FPGA interconnect: Routing resources, Elmore's constant, RC delay and parasitic capacitance, FPGA design flow, Dedicated specialized components of FPGAs.
UNIT– III
FPGA physical design, CAD tools, Power dissipation, FPGA Partitioning, Partitioning methods. Floor planning:I/O,Power and clock planning, Low-level design entry.
UNIT– IV
Placement and Routing: Placement algorithms: Min-cut based placement,Iterative Improvement and simulated annealing. Routing: introduction,Global routing:Global routing methods, Back-annotation. Detailed Routing: Channel density, Segmented channel routing,Mazerouting,Clock and power routing,Circuit extraction and DRC.

UNIT– V
Verification and Testing: Verification: Logic simulation, Design validation, Timing verification.Testing concepts: Failures, mechanism and faults, and fault coverage. Design Applications: General Design issues, Counter Examples, Case study of adders and accumulator architectures with XilinxVivadotool.

Suggested Reading:

1	Michael John Sebastian Smith, "Application Specific Integrated Circuits", PearsonEducationAsia,3rd edition, 2001.
2	Pak and Chan, Samiha Mourad, "Digital Design using Field Programmable Gate Arrays",PearsonEducation,1st edition, 2009
3	S.Trimberger,Edr, "FieldProgrammableGateArrayTechnology",KluwerAcademicPublications,1994.
4	John V. Oldfield, Richard C Dore, "Field Programmable Gate Arrays", WileyPublications.
5	CliveMaxfield, "TheDesignWarrior'sGuidetoFPGAs",Elsevier,2004.

ADVANCED DIGITAL SIGNAL PROCESSING

PE506EC

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits : 3
Prerequisites: Digital Signal Processing (PC408EC)

Course Objectives:

1.	To comprehend characteristics of discrete time signals and systems
2.	To analyze signals using various transform techniques
3.	To identify various factors involved in design of digital filters

Course Outcomes: On successful completion of the course, the students will be able to

1.	design FIR and IIR filters structure for different applications
2.	design FIR and IIR type digital filters with error analysis
3.	interpret various DSP algorithms for arithmetic operations
4.	identify filter structures and evaluate the coefficient quantization effects
5.	estimate power spectrum of signals using different methods

UNIT – I
Digital Filter Structures:FIR filters - Direct form, Cascade form, Frequency sampling, Lattice IIR filter - Direct form I, Direct form II, Cascade form, Parallel form Lattice & Lattice loader, Quantization of filter coefficients - Sensitivity to Quantization of filter coefficients, Quantization of coefficients in FIR filters, Round off effects in digital filters - Limit cycle, scaling to prevent overflow.
UNIT – II
Digital Filter Design: Linear phase FIR filter, characteristic response, location of zeros, Design of FIR filter - Windowing, Frequency sampling, Design of IIR filters from Analog filters - Impulse invariance, Bilinear transformation, Matched z-transform. Spectral transformations of IIR filters – FIR filter design –based on Windowed Fourier series – design of FIR digital filters with least – mean square-error – constrained Least –square design of FIR digital filters.
UNIT – III
DSP Algorithm Implementation: Computation of the discrete Fourier transform, Number representation, arithmetic operations, handling of overflow, tunable digital filters, function approximation.
UNIT – IV
Analysis of Finite Word Length Effects: The Quantization process and errors, Quantization of fixed–point and floating–point Numbers, Analysis of coefficient Quantization effects, Analysis of Arithmetic Round-off errors, Dynamic range scaling, signal-to-noise in Low-order IIR filters, Low-Sensitivity Digital filter, Reduction of Product round-off errors feedback, Limit cycles in IIR digital filter, Round-off errors in FFT Algorithms.
UNIT – V
Power Spectrum Estimation: Estimation of spectra from finite duration observation signals, the Periodogram, Use DFT in power Spectral Estimation, Bartlett, Welch and Blackman, Tukey

methods, Comparison of performance of Non-Parametric Power Spectrum Estimation Methods. Parametric Method of Power Spectrum Estimation, Relationship between Auto-Correlation and Model Parameters, AR (Auto-Regressive) Process and Linear Prediction, Yule-Walker, Burg and Unconstrained Least Squares Methods, Sequential Estimation, Moving Average(MA) and ARMA Models.

Suggested Reading:

1	John G.Proakisand DimitrisG. Manolakis, "Digital Signal Processing-Principles,Algorithms and Applications", PHI, 3rdedition, 2002.
2	AlanV.Oppenheim and Ronald W.Schafer , "DiscreteTimeSignalProcessing" 3rdEdition, PHIPublications.
3	Glenn Zelniker,Fred J. Taylor, "AdvancedDigitalSignalProcessing-TheoryandApplications", CRC Press.
4	Li Tan, "Digital Signal Processing-Fundamentals and Applications", Academic Press Publications.
5	nanuel C. Ifeacher, Barrie. W. Jervis, "DSP – A Practical Approach", 2ndedition, Pearson Education.

CMOS ANALOG IC DESIGN

PE507EC

Instruction: 3 periods per week *Duration of SEE:- 3hours*
CIE: 30 marks *SEE:- 70 Marks*
Credits: 3
Prerequisites: VLSI Design (PC414EC)

Course Objectives:

1. To develop models of basic CMOS amplifiers and Learn the concepts of advanced current mirrors.
2. To design and analyse differential amplifier and two-stage operational amplifier.
3. To study the Bandgap Reference circuits.

Course Outcomes: On successful completion of the course, the students will be able to

1. describe the small signal model of MOSFET and analyse the Single Stage Amplifiers.
2. analyse the differential amplifiers with MOS Loads and Current mirror loads.
3. analyse the frequency response of amplifiers.
4. design a fully compensated opamp and analyse the frequency response of the opamp.
5. analyse the bandgap reference circuits.

UNIT I
Basic MOS device Physics: MOS FET device I/V characteristics, second order effects, MOS device Capacitances, MOS small signal Model, NMOS verses PMOS devices. **Single stage amplifiers:** Common source stage with resistive load, diode connected load, triode load, current source load, CS stage with source degeneration, source follower, Common Gate stage, Gain boosting techniques, Cascode, folded cascode, choice of device models.
UNIT –II
Differential amplifiers: Single ended and differential operation, Basic differential pair, Common mode response, Differential amplifier with MOS loads, Gilbert cell. **Passive and Active Current mirrors:** Basic Current mirrors, Cascode Current mirrors, Active Current mirrors, Wilson and Widlar current mirrors
UNIT- III
Frequency Response of Amplifiers: General Considerations, Common-Source Stage, Source Followers, Common–Gate Stage, Cascode Stage, Differential Pair.
UNIT – IV
Operational Amplifiers: General Considerations, One stage Op-amp, 2- stage OP amp, Gain Boosting, Common mode feedback, Phase Margin, Frequency compensation.
UNIT –V
Band Gap References: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT current generation.

Suggested Reading:

1.	Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw Hill. 2002
2.	Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000
3.	David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004
4.	Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, International Second Edition/Indian Edition, 2010.
5.	Paul.R. Gray & Robert G. Major, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004

IoT SYSTEM DESIGN AND APPLICATIONS

PE508EC

Instruction: 3periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits : 3
Prerequisites:MicroProcessor and MicroController(PC409EC)

Course Objectives:

1. To discuss fundamentals of IoT and its applications and requisite infrastructure.
2. To describe Internet principles and architecture and applications relevant to IoT.
3. To discuss private and security aspects of IoT system.

Course Outcomes: On successful completion of the course, the students will be able to

1. understand IoT technology and research directions.
2. comprehend various protocols and architecture of IoT
3. design simple IoT systems with IoT reference model
4. understand the various applications of IoT
5. comprehend the different privacy and security approaches at IoT.

UNIT – I
IoT & Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics.
UNIT – II
M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.
UNIT – III
IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.
UNIT – IV
IoT Applications: Introduction, IoT Physical Devices and Endpoints: Raspberry Pi, Interfaces of Pi, Programming pi - Controlling LED and LDR using Pi, Opinions on IoT Application and Value for Industry, Home Management, Smart Cities, Smart Environment, Smart Energy, Smart Retail and Logistics, Smart Agriculture and Industry, Smart Industry and eHealth.
UNIT – V
Internet of Things Privacy: Security and Governance Introduction, Overview of Governance, Privacy and Security Issues, Contribution from FP7 Projects, Security, Privacy and Trust in IoT-Data-Platforms for Smart Cities, First Steps Towards a Secure Platform, Smartie Approach. Data Aggregation for the IoT in Smart Cities, Security

Suggested Reading:

1	Vijay Madisetti and ArshdeepBahga, 'Internet of Things (A Hands-on-Approach)',1st edition, VPT, 2014.
2	Francis daCosta, 'Rethinking the Internet of Things: A Scalable Approach to Connecting Everything', 1st edition, Apress Publications, 2013.
3	Cuno Pfister, 'Getting Started with the Internet of Things', O'Reilly Media, 2011.
4	Adrian McEwen, Hakim Cassimally, "Designing the Internet of Things", Wiley India Publishers,2014.
5	Vermesan, Ovidiu and Peter Friess, eds. Internet of things: converging technologies for smart environments and integrated ecosystems. River publishers, 2013.

OPEN ELECTIVE-1

PRINCIPLES OF ELECTRONIC COMMUNICATION

OE601EC

Instruction:3periodsperweek *Duration of SEE:3 hours*
CIE:30marksSEE:70 marks
Credits: 3

Course Objectives:

1. To provide an introduction to fundamental concepts in the understanding of communications systems.
2.To describe the network model and some of the network layers including physical layer, data link layer ,network layer and transport layer.
3.To discuss the evolution of wireless systems and current wireless technologies.

Course Outcomes: On successful completion of the course, the students will be able to

1.understandthe working of analog and digital communication systems.
2.explain the OSI network model and the working of data transmission.
3.describe the evolution of communication technologies from traditional telephony systems to modern wireless communication systems.
4.differentiate between analog and digital modulation techniques
5.understand the optical fiber communication link, structure, propagation and transmission properties.

UNIT– I
Introduction to Communication Systems: Electromagnetic Frequency Spectrum, Signal and its representation, Elements of Electronic Communications System, Types of Communication Channels. Signal Transmission Concepts: Baseband transmission and Broadband transmission, Communication Parameters: Transmitted power, Channel bandwidth and Noise, Need for modulation Signal Radiation and Propagation: Principle of electromagnetic radiation, Types of Antennas, Antenna Parameters and Mechanisms of Propagation.
UNIT– II
Analog and Digital Communications: Amplitude modulation and demodulation, FM modulation and demodulation, Digital converters, Digital modulation schemes– ASK,FSK,PSK,QPSK, Digital demodulation.
UNIT– III
Data Communication and Networking: Network Models, OSI Model, Data Link Layer–Media Access control, Ethernet, Network Layer–Internet Protocol(IPv4/IPv6),Transport Layer– TCP,UDP.
UNIT-IV
Telecommunication Systems: Telephones, Telephone system, Paging systems, Internet Telephony. Optical Communications: Optical Principles, Optical Communication Systems, Fiber–Optic Cables, Optical Transmitters & Receivers, Wavelength Division Multiplexing.
UNIT-V
Wireless Communications: Evolution of Wireless Systems: AMPS,GSM,CDMA,WCDMA,OFDM.Current Wireless Technologies: Wireless LAN, Bluetooth, PAN and ZigBee, Infrared wireless, RFID communication, UWB, Wireless mesh networks,Vehicular adhoc networks.

Suggested Reading:

1	LouisE.Frenzel, "PrinciplesofElectronicCommunicationSystems",3rdedition,McGrawHill,2008.
2	BehrouzA. Forouzan, "DataCommunicationsandNetworking",5thedition,TMH,2012.
3	George Kennedy, Bernard Davis, "ElectronicCommunicationsystems",4thedition,McGrawHill,1999.
4	RappaportT.S.,"Wirelesscommunications",2ndedition,PearsonEducation,2010.
5	Wayne Tomasi, "Advanced Electronic Communications Systems", 6thedition, Pearson Education.

DIGITAL SYSTEM DESIGN USING VERILOG HDL

OE602EC

Instruction:3periods perweek *Duration of SEE: 3 hours*
CIE:30 marks *SEE:70marks*
Credits:3

Course Objectives:

1.To familiarize with various modeling styles: structural, dataflow and behavioral of Verilog HDL.
2.To develop combinational and sequential circuits using various modeling styles of Verilog HDL.
3.To review the implementation of Verilog HDL Modeling using real time examples.

Course Outcomes: On successful completion of the course, the students will be able to

1.implement and distinguish different Verilog HDL modeling styles
2.construct and analyze Verilog HDL models of combinational and sequential circuits.
3.design and develop Verilog HDL modeling and test bench for digital systems for the given specifications.
4.outline FPGA design flow and timing analysis.
5.understandtherealworlddesignexamples such as UART, timers, and CPUs.

UNIT-I
Structural modeling:Overview of Digital Design with Verilog HDL,Basic concepts,modules and ports, gate-level modeling, hazards and design examples.
UNIT-II
Data flow and Switch level modeling: data flow modeling, operands and operators.Switch Level Modeling:CMOS switches and bidirectional switches and design examples.
UNIT-III
Behavioral Modeling: Structured Procedures, Procedural Assignments, Timing Controls,Conditional Statements,multi-way branching,Loops,Sequential and Parallel blocks, Generate blocks. Combinational, sequential logic modules and design examples.
UNIT-IV
Synthesis and Verification: Tasks and Functions: Differences between Tasks and Functions. Verilog HDL synthesis, Application Specific IC (ASIC) and Field Programmable Gate Array(FPGA)designflow.Verification:TiminganalysisandTestbenchdesign.Designexamples.
UNIT-V
Real time implementations: Fixed-Point Arithmetic modules:Addition, Multiplication, Division, Arithmetic and Logic Unit (ALU), Timer, Universal Asynchronous Receiver and Transmitter(UART),CPU design: Datapath and control units.

Suggested Reading:

1.	SameerPalnitkar, "Verilog HDL AGuide to Digital Design and Synthesis", 2nd edition,Pearson Education,2006.
2.	Ming-BoLin,"DigitalSystemDesignsandPractices:UsingVerilogHDLandFPGA",WileyIndiaeditio n,2008.
3.	J. Bhasker, AVerilogHDLPrimer,2nd edition, BSPublications, 2001.
4.	CharlesRoth,Lizy.K.John,ByeongKilLee,-Digital SystemsDesignUsingVerilog,1st edition,CengageLearning, 2015.
5.	T.R.Padmanabhan,B.BalaTripuraSundari, "DesignthroughVerilogHDL" ,Studentedition,Wiley Publishers,2008.

COMMUNICATION SYSTEMS LAB

PC458EC

Instruction:2periodsperweek *Duration of SEE:3 hours*
CIE:25marks *SEE:50 marks*
Credits:1

Course Objectives:

1.To demonstrate AM, FM, Mixer, PAM, PWM, PPM and multiplexing techniques.
2.To understand and simulate digital modulation (i.e., ASK, FSK, BPSK, QPSK) generation.
3.To model analog, pulse modulation, PCM, Delta and Digital modulation techniques using CAD tools.

Course Outcomes: On successful completion of the course, the students will be able to

1.understand and simulate modulation and demodulation of AM and FM.
2.construct and understand the need for pre-emphasis and de-emphasis at the transmitter and receiver respectively.
3.simulate the PAM, PWM & PPM circuits.
4.understand generation and detection of baseband transmission (i.e., PCM, DM, and ADM) and bandpass transmission (i.e., ASK,FSK,PSK, MSK and QPSK)
5.understand the error control coding.

List of Experiments

PART-A

Analog Communication

1. Amplitude Modulation and Demodulation.
2. Frequency Modulation and Demodulation.
3. Pre-emphasis and De-emphasis and plot the frequency response.
4. Multiplexing Techniques (FDM and TDM).
5. Mixer Characteristics and plot the frequency response.
6. Verification of Sampling Theorem.
7. PWM, PPM generation and detection.
8. Generation and Detection of AM, FM, PAM, PWM, PPM modulation techniques using MATLAB/Simulink/Lab-view.

PART-B

Digital Communication

1. PCM modulation and demodulation.
2. Channel encoding and decoding.
3. Linear and Adaptive Delta Modulation and Demodulation.
4. ASK generation and Detection.
5. FSK and Minimum Shift Keying generation and Detection.
6. ASK generation and Detection.
7. Generation and Detection of PCM, Delta modulation and Digital modulation schemes (ASK, FSK, BPSK, QPSK) by using MATLAB/Simulink/Lab-view.

NOTE:

1. At least ten experiments to be conducted in the semester.
2. Minimum of 5 from Part A and 5 from Part B is compulsory.

DIGITAL INTEGRATED CIRCUITS DESIGN LAB

PC459EC

Instruction: 2 periods per week *Duration of SEE:- 3hours*
CIE: 25 marks *SEE:- 50 Marks*
Credits: 1

Course Objectives:

1. To develop verilog HDL code for digital circuits using gate level, data flow and behavioral, modeling and Verify the design block using stimulus.
2. To study the VLSI CAD tools.
3. To implement transistor level circuits.

Course Outcomes: On successful completion of the course, the students will be able to

1.write the Verilog HDL programs in gate level and data flow modeling.
2.implement combinational and sequential circuits using Verilog.
3.analyse digital circuits using VLSI CAD tools like Mentor Graphics / Cadence
4.design CMOS circuits like basic gates, adders at the transistor level
5. implement the layout of simple CMOS circuits like inverter and basic gates.

List of Experiments:

Part-A

Write the Code using Verilog and simulate the following:

1. Write structural and dataflow Verilog HDL models for
a) 4-bit ripple carry adder.
b) 4-bit carry Adder – cum Subtractor.
c) 2-digit BCD adder / subtractor.
d) 4-bit carry look ahead adder
e) 4-bit comparator

2. Write a Verilog HDL program in behavioral model for
a) 8:1 multiplexer
b) 3:8 decoder
c) 8:3 encoder
d) 8 bit parity generator and checker

3. Write a Verilog HDL program in Hierarchical structural model for
a) 16:1 multiplexer realization using 4:1 multiplexer
b) 3:8 decoder realization through 2:4 decoder
c) 8-bit comparator using 4-bit comparators and additional logic

4. Write a Verilog HDL program in behavioral model for D,T and JK flip flops, shift registers and counters.

5. Write a Verilog HDL program in structural and behavioral models for
a) 8 bit asynchronous up-down counter b) 8 bit synchronous up-down counter

6.Write a Verilog HDL program for 4 bit sequence detector through Moore state machines
7.Write a Verilog HDL program for 4 bit sequence detector through Mealy state machines

PART-B

Transistor Level implementation of CMOS circuits using VLSI CAD tool

1. Basic Logic Gates: Inverter, NAND and NOR
2. Half Adder and Full Adder
3. 2:1 Multiplexer and 4:1 Multiplexer using 2:1 Multiplexer
4. one bit comparator and four-bit magnitude comparator using one bit comparator
5. Implement the Layout of CMOS Inverter.
6. Implement the Layout of CMOS NAND.

Note:

2. A total of 10 experiments must be completed in the semester.
3. Minimum of 5 experiments from Part-A and 5 from Part-B is compulsory.

DATA COMMUNICATION AND COMPUTER NETWORKSLAB

PC460EC

Instruction:2periodsperweek *Duration ofSEE: 3hours*
CIE:25marks *SEE:50marks*
Credits: 1

Objectives:

1. To understand a conceptual foundation for the study of data communications using the open Systems interconnect (OSI) model for layered architecture.
2. To understand the performance of data link layer protocol HDLC.
3. To understand network layer routing protocols and algorithms.

Outcomes: On successful completion of the course, the students will be able to

1.understand the working of various network topologies in circuit and packet switching.
2. implement HDLC protocol and significance of MAC protocols.
3. understand the network routing protocols and the associated algorithms.
4. understand the transport layer working with TCP, and UDP.
5. implement network scenario and obtain its performance evaluation.

List of Experiments:

PART-A

Design and implement the following experiments using C Compiler and packet tracer software

1. Study of network devices in detail.
2. A HDLC frame to perform the following.
   i.Bit stuffing
   ii.Character stuffing.
3. Distance vector algorithm and find path for transmission.
4. Dijkstra's algorithm to compute the shortest routing path.
5. Simulation of network topologies.
6. Configuration of a network using different routing protocols.

PARTB

Simulation using NS2/ NS3/ NCTUNS/ NetSim or any other equivalent tool in Linux OS.

1.Point to point network with four nodes and duplex links between them. Analyse the network performance by setting the queue size and varying the bandwidth.
2.Four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent byTCP/UDP.
3.Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4.Implement Ethernet LAN using n nodes and assignment of multiple traffic to obtain congestion window for different sources/destinations.
5.ESS with transmission nodes in Wireless LAN and study of performance parameters.
6.Implementation of Link state routing algorithm.

NOTE:

1. At least ten experiments to be conducted in the semester.
2. Minimum of 5 from Part A and 5 from Part B is compulsory.

SUMMER INTERNSHIP

PW702EC

Instruction: NA *Duration of SEE: NA*
CIE: 50 marks *SEE: NA*
Credits : 2

Course Objectives:

1.	To enhance practical and professional skills.
2.	To provide training in soft skills and also train them in presenting seminars and technical report writing.
3.	To expose the students to industry practices and team work

Course Outcomes: On successful completion of the course, the students will be able to

1.	acquirepractical experience of software design and development, and coding practices within Industrial/R&D Environments.
2.	understand working practices within Industrial/R&D Environments
3.	prepare reports and deliver effective presentation.
4.	demonstrate effective written and oral communication skills
5.	innovate in various engineering disciplines and nurture their entrepreneurial ideas.

Summer Internship is introduced as part of the curriculum for encouraging students to work on problems of interest to industries. A batch of three students will be attached to a person from the Government or Private Organisations/Computer Industry/Software Companies/R&D Organization for a period of 4 to 6 weeks. This will be during the summer vacation following the completion of the III-year Course. One faculty coordinator will also be attached to the group of 3 students to monitor the progress and to interact with the industry co-ordinate (person from industry).
The course schedule will depend on the specific internship/training experience. The typical time per topic will vary depending on the internship
- Overview of company/project
- Safety training
- Discussions with project teams
- Background research, review of documents, white papers, and scientific papers
- Planning, designing, and reviewing the planned work
- Executing the plans
- Documenting progress, experiments, and other technical documentation
- Further team discussions to discuss results
- Final report writing and presentation

After the completion of the project, each student will be required to:
1. Submit a brief technical report on the project executed and
2. Present the work through a seminar talk (to be organized by the Department)

Award of internal marks are to be based on the performance of the students at the workplace and awarded by industry guide and internal guide (25 Marks) followed by presentation before the

committee constituted by the department (25 Marks). One faculty member will co-ordinate the overall activity of Industry Attachment Program.

Note: Students have to undergo summer internship of 4 to 6 weeks at the end of semester VI and credits will be awarded after evaluation in VII semester.